REMARKS

In the Official Action mailed on **June 4, 2004,** the Examiner reviewed claims 1-20. Claims 1-18 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Claims 1 and 10 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 19 and 20 were rejected under 35 U.S.C. §102(e) as being anticipated by Gonzales et al. (USPN 6,101,614, hereinafter "Gonzales"). Claims 19 and 20 were rejected under 35 U.S.C. §102(e) as being anticipated by Epsie et al. (USPN 6,076,183, hereinafter "Epsie").

Rejections under 35 U.S.C. §112, first paragraph

Claims 1-18 were rejected as failing to comply with the enablement requirement.

Applicant has amended independent claims 1 and 10 to clarify that it is the data that is corrected and checked out to the processor cache rather than the memory location. These amendments find support in page 9, lines 19-27 of the instant application.

Rejections under 35 U.S.C. §112, second paragraph

Claims 1 and 10 were rejected as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicant has amended independent claims 1 and 10 to clarify that the data in a memory location and/or a corresponding cache line is examined and if the data is in error, the errors are corrected. These amendments find support in page 9, lines 19-27 of the instant application.

Rejections under 35 U.S.C. §102(e)

Claims 19 and 20 were rejected as being anticipated by Gonzales. Claims 19 and 20 were rejected as being anticipated by Epsie. Applicant respectfully points out that both Gonzales and Epsie teach scrubbing main memory to **correct errors in the main memory** (see Gonzales, col. 3, lines 1-34 and 41-50; also see Epsie, FIGs. 4-5, col. 2, line 30 to col. 4 and col. 8, line 37 to col. 9, line 55).

In contrast, the present invention is directed to marking locations in main memory when the data from the location has been checked out to cache. In this way, when the memory location is subsequently being scrubbed, if the system determines that the memory location is marked and has hence been checked out to the cache, the system recovers the data from cache, corrects it if necessary in the cache, and returns the data to main memory (see page 8, line 21 to page 9, line 11 of the instant application). Note that this technique **corrects errors in both the cache and the main memory**. The prior art does not correct errors in the cache.

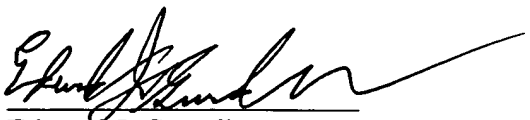
Accordingly, Applicant has amended independent claim 19 to clarify that the present invention marks locations in main memory when the data from the location has been checked out to cache, so that when the memory location is subsequently being scrubbed, if the memory location is marked and has hence been checked out to the cache, the system recovers the data from cache, corrects it if necessary in the cache, and returns the data to main memory. These amendments find support on page 8, line 21 to page 9, line 11 of the instant application

Hence, Applicant respectfully submits that independent claims 1, 10, and 19 as presently amended are in condition for allowance. Applicant also submits that claims 2-9, which depend upon claim 1, claims 11-18, which depend upon claim 10, and claim 20, which depends upon claim 19 are for the same reasons in condition for allowance and for reasons of the unique combinations recited in such claims.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

By 

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